SESSION 12 – TAPA I
Device Characterization/Modeling

Wednesday, June 16, 1:30 p.m.
Chairpersons: J. Wu, Texas Instruments
T. Hiramoto, University of Tokyo

**12.1 — 1:30 p.m.**
**Rigorous Mathematical Calculation of p- and n-Mobility as Functions of Mechanical Stress, Electric Field, Current Direction and Substrate Indices for Scaled CMOS Designing,** T. Okada and H. Yoshimura*, Toshiba Corporation, Kawasaki, Japan, *Toshiba Corporation, Yokohama, Japan

Mobility enhancement attempts and imbalance discussion in p- and n- mobility have been still heated up in order to design scaled CMOS including strained silicon, germanium, and silicon substrate as well. However, there has been still remaining physical aspects unresolved such as quantitative understanding of scattering rate characteristics and effective mass in anisotropic energy diagrams and so on. Here we have conducted developing rigorous physical equation of Schrödinger based wave functions without any fitting parameters, and we herein provide new three dimensional output chart in terms of mechanical stress, external electric field, surface orientation, current direction. We also report new demonstration of scaled CMOS design using materials optimization.

**12.2 — 1:55 p.m.**
**Understanding Stress Enhanced Performance in Intel 90nm CMOS Technology,** M.D. Giles, M. Armstrong, C. Auth, S.M. Cea, T. Ghani, T. Hoffmann, R. Kotlyar, P. Matagne, K. Mistry, R. Nagisetty, B. Obradovic, R. Shaheed, L. Shifren, M. Stettler, S. Tyagi, X. Wang, C. Weber, K. Zawadzki, Intel Corporation, Hillsboro, OR

A hierarchical, model-based understanding of stress-induced device performance gain is presented for Intel's novel strained transistor architecture incorporating epitaxially grown strained SiGe source-drain regions for PMOS and a highly tensile silicon nitride capping layer for NMOS. The key physical effects are shown underlying the large benefit seen in this architecture from applying uniaxial PMOS channel stress and the importance of the vertical stress component in NMOS performance gain.

**12.3 — 2:20 p.m.**
**Direct Measurement of Stress Dependent Inversion Layer Mobility Using a Novel Test Structure,** T. Okagaki, M. Tanizawa, T. Uchida, T. Kunikiyo, K. Sonoda, M. Igarashi, K. Ishikawa, T. Takeda*, P. Lee* and G. Yokomizo*, Renesas Technology Corporation, Hyogo, Japan, *Renesas Technology Corporation, Tokyo, Japan

We propose a novel mobility measurement method which can be applied to industrial sized MOSFETs. The mobility variation caused by STI stress is evaluated directly. Extracted piezo resistance coefficients in the inversion layer are close to their counterparts in bulk silicon. Additionally, we have observed for the first time that the inversion layer mobility in <100> channel MOSFETs is less sensitive to the STI stress than that in <110> channel MOSFETs.

**12.4 — 2:45 p.m.**
**Direct Measurement of Barrier Height at the $HfO_2$/poly-Si Interface:Band Structure and Local Effects,** L. Pantisano, P.J. Chen*, V. Afanas'ev**, L.Å. Ragnarsson, G. .Pourtois and G. Groesenekenen, IMEC, Leuven, Belgium, *Texas Instruments, **KU Leuven, Belgium

The presence of traces of HfO2 at the poly-Si/SiO2 interface creates (amphoteric) defects, which induce a spatially nonuniform change in the barrier height, regardless of poly-Si doping type. The screening of such Hf-induced defects produces a built-in Coulomb-like field, which negatively impacts the channel electron mobility and the poly-Si gate depletion. By using a VBET-based approach, for the first time a similar change in barrier height is demonstrated on Hf-based stacks with arbitrary compositions with poly-Si as gate electrode.